CLAIMS

What is claimed is:

1. (Currently amended) A floating gate flash memory device comprising:

a) a substrate comprising a source region, a drain region, and a channel region positioned therebetween;

b) a reverse tunnel dielectric layer;

c) a stack gate comprising a floating gate electrode, hard mask spacers, and at least one of sidewall/spacers, second sidewalls or a barrier layer, wherein the floating gate electrode is positioned above the channel region, with the floating gate electrode separated from the hard mask spacers by the at least one of sidewall/spacers, second sidewalls or a barrier layer, wherein the floating gate electrode is separated from the channel region by the reverse tunnel dielectric layer; and

d) a control gate electrode positioned above the floating gate electrode and separated from the floating gate electrode by an interpoly dielectric layer.

2. (Currently amended) The device of claim 1, wherein the floating gate electrode is a metal floating gate electrode.

3. (Currently amended) The device of claim 2, wherein the metal floating gate electrode comprises one or more of RuO_2, Ru, Rh, Pd, Os, Ir and Pt, mixtures and alloys thereof and alloys comprising one or more of Ru, Rh, Pd, Os, Ir and Pt.

4. (Currently amended) The device of claim 2, wherein the metal floating gate electrode is separated from the reverse tunnel dielectric layer by the barrier layer.

5. (Original) The device of claim 1, wherein the barrier layer comprises at least one layer containing at least one of RuTiN, TiN, TaN, TaSiN, TiW, WN, or a mixture or composite thereof.

6. (Original) The device of claim 1, wherein the stack gate comprises both the second sidewalls and the barrier layer.

7. (Original) The device of claim 1, further comprising shallow trench isolation structures adjacent the source region and the drain region.

8. (Currently amended) A floating gate flash memory device comprising:

a) a substrate comprising a source region, a drain region, and a channel region positioned therebetween;

b) a stack gate comprising a metal floating gate electrode, hard mask spacers, sidewall/spacers and a barrier layer, wherein the barrier layer includes sidewalls adjacent the metal floating gate electrode, the sidewall/spacers are between the metal floating gate electrode and the hard mask spacers, the metal floating gate electrode is positioned above the barrier layer and the stack gate is separated from the channel region by a pad dielectric layer; and

c) a control gate electrode positioned above the metal floating gate electrode and separated from the metal floating gate electrode by an interpoly dielectric layer.

9. (Original) The floating gate flash memory device of claim 8, further comprising second sidewalls.

10. (Currently amended) The device of claim 8, wherein the metal floating gate electrode comprises one or more of RuO_2, Ru, Rh, Pd, Os, Ir and Pt, mixtures and alloys thereof and alloys comprising one or more of Ru, Rh, Pd, Os, Ir and Pt.

11. (Original) The device of claim 8, wherein the barrier layer comprises at least one layer containing at least one of RuTiN, TiN, TaN, TaSiN, TiW, WN, or a mixture or composite thereof.

12. (Original) The device of claim 8, further comprising shallow trench isolation structures adjacent the source region and the drain region.

13. (Currently amended) A floating gate flash memory device comprising:

a) a substrate comprising a source region, a drain region, and a channel region positioned therebetween;

b) a stack gate comprising a metal floating gate electrode, hard mask spacers and a barrier layer, wherein the barrier layer includes sidewalls separating the metal floating gate electrode from the hard mask spacers, the metal floating gate electrode is positioned above the barrier layer and the stack gate is separated from the channel region by a pad dielectric layer; and

c) a control gate electrode positioned above the metal floating gate electrode and separated from the metal floating gate electrode by an interpoly dielectric layer.

14. (Currently amended) The device of claim 13, wherein the metal floating gate electrode comprises one or more of RuO_2, Ru, Rh, Pd, Os, Ir and Pt, mixtures and alloys thereof and alloys comprising one or more of Ru, Rh, Pd, Os, Ir and Pt.

15. (Original) The device of claim 13, wherein the barrier layer comprises at least one layer containing at least one of RuTiN, TiN, TaN, TaSiN, TiW, WN, or a mixture or composite thereof.

16. (Original) The device of claim 13, further comprising shallow trench isolation structures adjacent the source region and the drain region.

17. (Currently amended) A floating gate flash memory device comprising:

a) a substrate comprising a source region, a drain region, and a channel region positioned therebetween;

b) a reverse tunnel dielectric layer;

c) a stack gate comprising a metal floating gate electrode, hard mask spacers, and a barrier layer, wherein the barrier layer includes sidewalls separating the metal floating gate electrode from the hard mask spacers, the metal floating gate electrode is positioned above the barrier layer and the stack gate is separated from the channel region by the reverse tunnel dielectric layer; and

d) a control gate electrode positioned above the metal floating gate electrode and separated from the metal floating gate electrode by an interpoly dielectric layer.

18. (Currently amended) The device of claim 17, wherein the metal floating gate electrode comprises one or more of RuO_2, Ru, Rh, Pd, Os, Ir and Pt, mixtures and alloys thereof and alloys comprising one or more of Ru, Rh, Pd, Os, Ir and Pt.

19. (Original) The device of claim 17, wherein the barrier layer comprises at least one layer containing at least one of RuTiN, TiN, TaN, TaSiN, TiW, WN, or a mixture or composite thereof.

20. (Original) The device of claim 17, further comprising shallow trench isolation structures adjacent the source region and the drain region.